AMENDMENTS TO THE CLAIMS

1. – 5. (Cancelled)

6. (Previously Presented) An input level translator circuit comprising:

a first pass circuit that is coupled to a full-range node, to a first bias node, and to a high-range node;

a second pass circuit that is coupled to the full-range node, to a second bias node, and to a low-range node;

a first shunt circuit that is coupled between the first bias node and the high-range node; and

a second shunt circuit that is coupled between the second bias node and the low-range node, wherein

the first shunt circuit comprises a transistor that has:

a gate that is coupled to the full-range node,

a source that is coupled to the high-range node, and

a drain that is coupled to the first bias node.

7. (Original) The input level translator circuit of claim 6, wherein

the second shunt circuit comprises a transistor that has:

a gate that is coupled to the full-range node,

a source that is coupled to the low-range node, and

a drain that is coupled to the second bias node.

8. – 20. (Cancelled)